



Gp 2875
ZFW
Gabara 80-7

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): T.J. Gabara et al.

Case: 80-7

Serial No.: 10/079,447

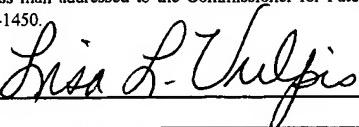
Filing Date: February 20, 2002

Group: 2825

Examiner: Granvill D. Lee

Title: Method for Modeling Noise Emitted by Digital Circuits

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature:  Date: July 29, 2004

TRANSMITTAL LETTER

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith is the following document relating to the above-identified patent application:

(1) Response to Office Action.

There is no additional fee due in conjunction with the response. In the event of any non-payment or improper payment of a required fee, the Commissioner is hereby authorized to charge or to credit **Ryan, Mason & Lewis, LLP Account No. 50-0762** as required to correct the error.

Respectfully submitted,



Date: July 29, 2004

Joseph B. Ryan
Attorney for Applicant(s)
Reg. No. 37,922
Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560
(516) 759-7517



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): T.J. Gabara et al.

Case: 80-7

Serial No.: 10/079,447

Filing Date: February 20, 2002

Group: 2825

Examiner: Granvill D. Lee

Title: Method for Modeling Noise Emitted by Digital Circuits

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature:

Date: July 29, 2004

RESPONSE TO OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The remarks below are submitted in response to the second non-final Office Action dated May 12, 2004 in the above-identified application.

REMARKS

The present application was filed on February 20, 2002 with claims 1-26, claiming the priority of U.S. provisional patent application Serial No. 60/270,263 filed February 21, 2001. Claims 1-26 are currently pending in the application. Claims 1, 5, 9 and 18 are the independent claims.

In the Office Action, claims 1 and 5 are rejected under 35 U.S.C. §102(e) as being anticipated by Heijningen et al., *Analysis and Experimental Verification of Digital Substrate Noise Generation for Epi-Type Substrates*, IEEE Journal of Solid-State Circuits, Vol. 35, No. 7 (July 2000) (hereinafter “Heijningen”). In addition, claim 9 is rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Pat. No. 6,135,649 to Feldmann et al. (hereinafter “Feldmann”). Finally, claims 9-11, 13, 18-20, 22